60-GHz Flip-Chip Assembled MIC Design Considering Chip–Substrate Effect

Yukari Arai, Masakatsu Sato, Hiromi T. Yamada, Tomoji Hamada, Kiyoshi Nagai, and Hiroki I. Fujishiro

***Abstract*— In this paper, 60-GHz microwave integrated circuits (MIC's) with flip-chip assembled 0.1-μm-gate GaAs pseudomorphic high electron-mobility transistors (p-HEMT's) are demonstrated. To clarify the millimeter-wave characteristics of the flip-chip assembled structure, the parameters for the assembly equivalent circuit are examined using three-dimensional (3-D) electromagnetic-field analysis. The analytical results indicate that the optimum height of the bump is 30 μm to minimize degradation of the millimeter-wave characteristics. A 60-GHz-band MIC two-stage amplifier and 30/60-GHz frequency doubler designed using the results of the field analysis have been fabricated. The amplifier has maximum gain of 12.8 dB at 58.6 GHz. $P_{1\,\mathrm{dB}}$ of 12.9 dBm has been obtained at 60 GHz. A 30/60-GHz frequency doubler has maximum conversion gain of 0.4 dB and fundamental frequency suppression of -23.0 dB at the input frequency of 30.4 GHz. Good agreement between the measured and the simulated results demonstrates the potential of the structure and design method.**

***Index Terms*—Circuit modeling, electromagnetic analysis, electron beam lithography, hybrid integrated circuits, integrated circuit modeling, millimeter-wave technology, millimeter-wave circuits, MODFET.**

I. Introduction

THESE DAYS, rapidly increasing demand for wireless communications and radar systems has resulted in much attention being given to the millimeter-wave region as new frequency resources. For this application, cost effectiveness and high yield of circuit fabrication are significant requirements as well as superior characteristics of the circuits.

There are two approaches to realize millimeter-wave circuits: microwave integrated circuits (MIC's) [1] and monolithic microwave integrated circuits (MMIC's) [2]. The MIC approach, where discrete transistors are assembled on dielectric circuit substrates, is advantageous compared to the MMIC approach because of the following factors.

1) The total semiconductor area required is much smaller.
2) Chips with acceptable characteristics can be selected during the assembly process.
3) Handling of dielectric substrates, upon which passive elements are fabricated, is much easier than handling of compound semiconductor chips.

These factors together will lead to design flexibility, high production yield, and low cost. On the other hand, in MMIC's, fabricating distributed circuit elements and active components together on the same semiconductor substrate not only renders the semiconductor chip size considerably larger, but also requires more complex fabrication processes such as via-hole etching, backside plating, interconnection process for additional layers, etc.

When assembling MIC's for operation at millimeter-wave frequencies, the use of flip-chip technology is preferable—almost necessary—due to its short and stable interconnection as compared with wire bonding.

In spite of the merits of flip-chip assembled MIC's for millimeter-wave applications, their use has been limited. This is partly because sufficiently accurate modeling of the assembly to enable circuit design has been considered difficult. One reason is that this modeling must include the influence of the electromagnetic interaction between the chip and the substrate [3], which we will call the "chip–substrate effect," since this interaction alters device parameters. Circuit modeling is not valid if this interaction is not properly accounted for. Another anticipated factor is that unpredictable assembly variations, such as bump height variation, smaller than that of wire bonding, but still present, may lead to uncertainty in modeling. In order to minimize the effect of assembly variations, precise control of the flip-chip assembly process or the selection of a structure for which the effect of these variations is sufficiently small is indispensable.

In this paper, we apply three-dimensional (3-D) field analysis to the flip-chip assembled MIC structure. The results of the analysis are incorporated into an equivalent circuit model for the assembly. This model provides a reasonable estimate of assembly-related parasitics, including the chip–substrate effect. From this analysis, we demonstrated a flip-chip assembly structure with suppressed chip–substrate effect and relatively low assembly variation influence.

We present flip-chip assembled MIC's with discrete GaAs pseudomorphic high electron-mobility transistors (p-HEMT's) on ceramic substrates at 60 GHz—the highest frequency ever reported for this type of structure. Through the demonstration of amplifier and frequency-doubler designs, we have confirmed the validity of the design method and the suitability of this MIC structure for application to millimeter-wave frequencies.

II. Analysis for Flip-Chip Assembly for Equivalent Circuit Modeling

Fig. 1(a) shows the structure of a discrete HEMT flip-chip assembled on a ceramic substrate.

The characteristics of the complete flip-chip assembled structure are not simply a combination of the individual

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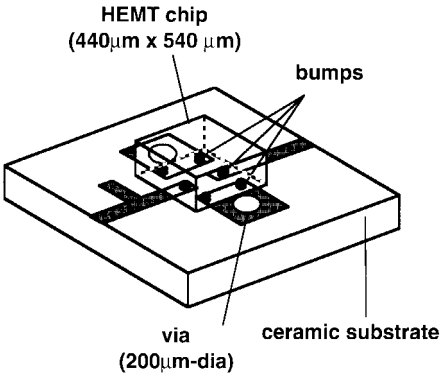
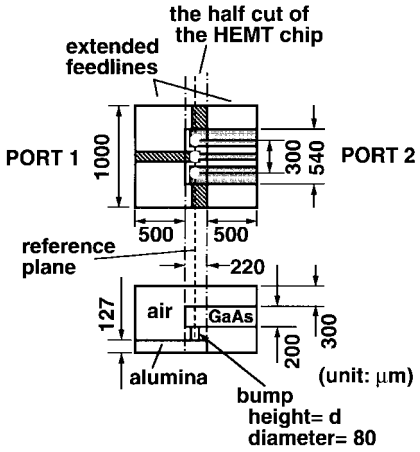


(a)



(b)

Fig. 1. (a) Structure of a discrete HEMT flip-chip assembled on a ceramic substrate. (b) Structure used in the electromagnetic-field analysis.

characteristics of each element because of electromagnetic effects due to the assembled structure. Therefore, accurate estimation of the assembly effect is important.

We performed electromagnetic simulation and incorporated the results into a circuit model for the assembly to realize 60-GHz-band MIC's.

A 3-D field analysis with HP-HFSS using the structure in Fig. 1(b) has been carried out. The half cut of an HEMT chip has been taken into consideration because the pad and feedline patterns for the drain side and the gate side on the HEMT are symmetrical. The feedline on the alumina substrate circuit (port 1) is microstrip, whereas that on the GaAs chip (port 2) is coplanar waveguide, being extended from the half-cut model in order to enable HFSS calculation. The grounded patterns on the alumina substrate are connected to the perfect electric conducting boundary wall instead of via-hole connecting to the backside. An air gap over the backside of the HEMT chip is introduced to avoid interaction between the chip and the analytical boundary.

The bump diameter is 80 μm and the bump height is d μm. S-parameters calculated with HFSS are de-embedded to the reference plane shown in Fig. 1(b), and then transformed into a Π-section equivalent circuit. Each admittance of the Π-circuit thus obtained is then converted into the lumped parameters C, L, R, and G [4].

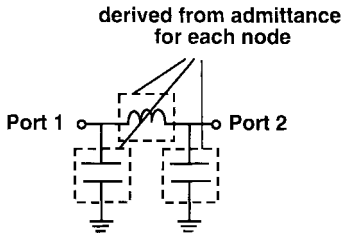


Fig. 2. Equivalent circuit model for flip-chip assembly.

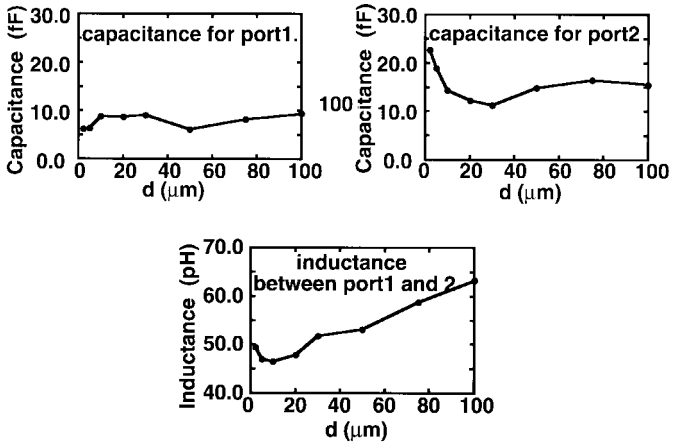


Fig. 3. Calculated lump element value versus bump height.

Using such an analytical procedure, simulated S-parameters at 60 GHz for various bump height d have been transformed into lumped elements. Neglecting the elements which have little influence on characteristics, the elements which prove to be critical are the capacitances for port 1 and port 2, and the inductance between ports. The equivalent circuit model for a single flip-chip assembly was then determined, as shown in Fig. 2.

Fig. 3 shows the simulated values of these essential lumped parameters versus bump height. Though the capacitance for port 1 is almost constant with respect to bump height, the capacitance for port 2 increases drastically for bump heights under 30 μm. In the case of the coplanar waveguide (port 2), electromagnetic-field expansion in the vertical direction is much larger than in the microstrip case (port 1), therefore, the chip–substrate interaction is increased. The excess portion of capacitance for shorter bump height, exclusively appearing in port 2, is thus estimated as the capacitance relating to the interaction between the chip and the substrate. From these results, a bump height of 30 μm, where the chip–substrate effect is suppressed and the capacitances for each port are relatively insensitive to bump height variation in assembly is suitable.

Fig. 4 shows the equivalent circuit model for a flip-chip assembled HEMT. Lumped-element values here are for the bump height of 30 μm.

To assess the validity of the assembled HEMT model, S-parameter simulation has been carried out. Fig. 5 illustrates the directly measured S-parameters of a flip-chip assembled HEMT (= measured) and simulated S-parameters using the circuit in Fig. 4, in which HEMT on-wafer measurement

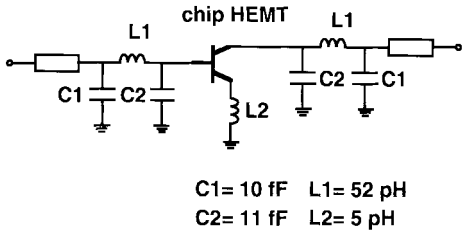


Fig. 4. Equivalent circuit model for flip-chip assembled HEMT.

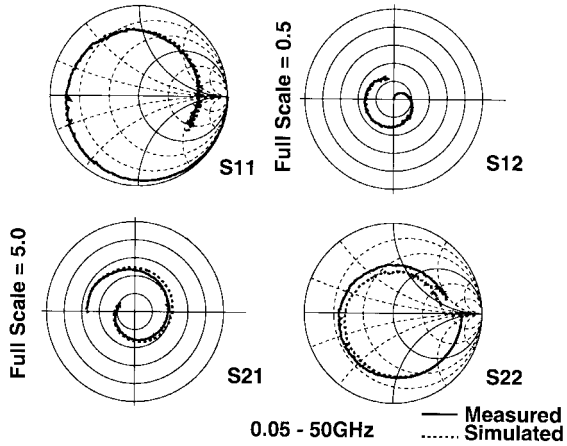


Fig. 5. Measured and simulated S-parameters for flip-chip assembled HEMT.

results are used (= simulated). The measurement of assembled HEMT was carried out with on-wafer test probes.

Good agreement between the two sets of S-parameter data is evidence of the accurate estimation of the developed flip-chip equivalent-circuit HEMT model. Based on this electromagnetic simulation and deviation of an equivalent circuit model for the flip-chip assembled HEMT, 60-GHz MIC circuit design and fabrication can be carried out.

III. Circuit-Design Procedure and Results

A. p-HEMT Structure and FET Root Model

For MIC application, we employed an InGaAs/AlGaAs double-doped p-HEMT [5], [6] which has a 0.10-μm-long and 100-μm-wide mushroom-shaped gate. Fig. 6 shows the cross-sectional view for the p-HEMT. Epitaxial layers have been grown with molecular-beam epitaxy (MBE). The bottom 0.10-μm patterns have been fabricated with direct-write electron-beam lithography, followed by use of i-line stepper lithography to define the upper 0.5-μm patterns. Wafers were thinned to a thickness of 200 μm and diced into discrete HEMT chips measuring 440 μm $\times$ 540 μm.

An FET Root model [7], used as the nonlinear FET model for the p-HEMT was extracted from on-wafer S-parameter measurements using HP IC-CAP software for the device evaluation and characterization.

Fig. 7 shows the drain I–V characteristics for a discrete p-HEMT. Directly measured I–V and that of the extracted FET Root model are compared.

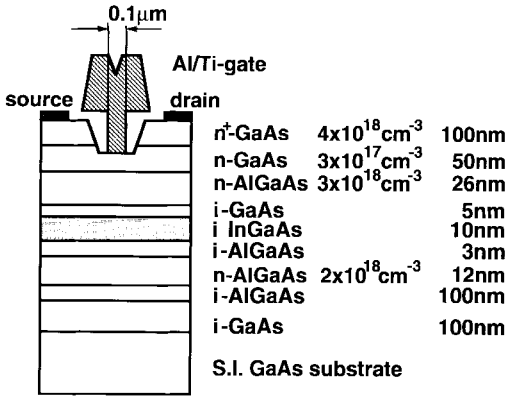


Fig. 6. Cross-sectional view of InGaAs/AlGaAs p-HEMT.

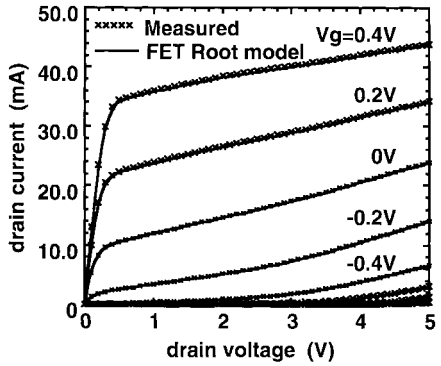


Fig. 7. Drain I–V characteristics for 0.1-μm-gate p-HEMT.

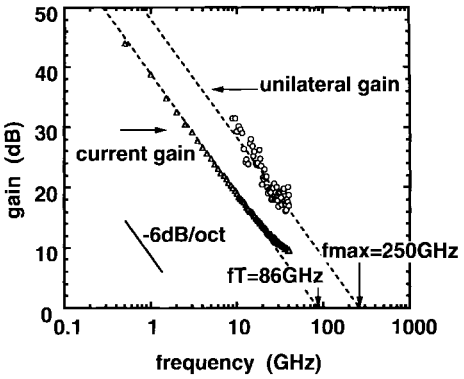


Fig. 8. Frequency characteristics for p-HEMT.

Fig. 8 illustrates the small-signal frequency characteristics for a discrete p-HEMT at a drain voltage $V_{\rm d} = 2$ V and drain current $I_{\rm d} = 25$ mA. Cutoff frequency (f_T) of 86 GHz and maximum oscillation frequency ($f_{\max}$) of 250 GHz have been derived from extrapolating current gain and unilateral gain with -6 dB/octave fitting curves.

By substituting the on-wafer extracted FET Root model into the "assembled HEMT" circuit of Fig. 4, we have obtained a flip-chip assembled HEMT model suitable for circuit design.

B. MIC Structure

Substrates for the MIC's are 1 cm $\times$ 1 cm, 127-μm-thick alumina ceramic with a relative dielectric coefficient of 9.8. Microstrip line circuits are patterned with 2-μm-thick gold

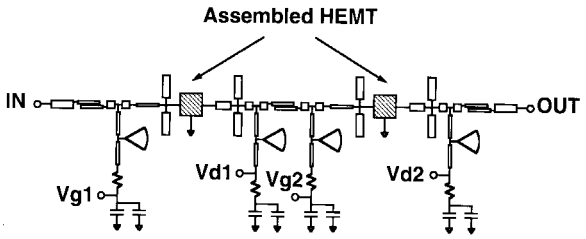


Fig. 9. Circuit diagram of 60-GHz two-stage cascade amplifier.

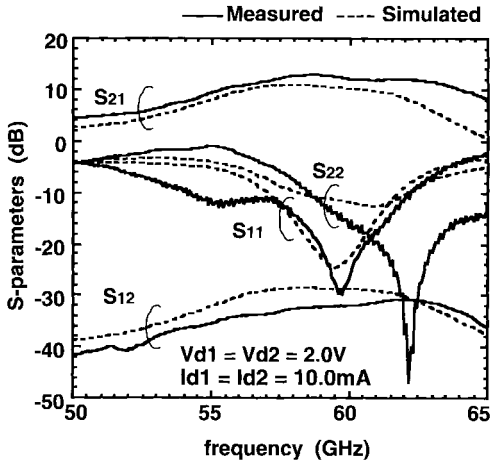


Fig. 10. Measured and simulated frequency characteristics of 60-GHz two-stage amplifier.

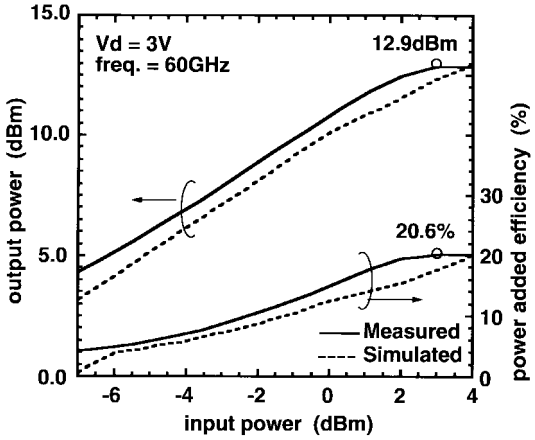


Fig. 11. Power characteristics of 60-GHz two-stage amplifier.

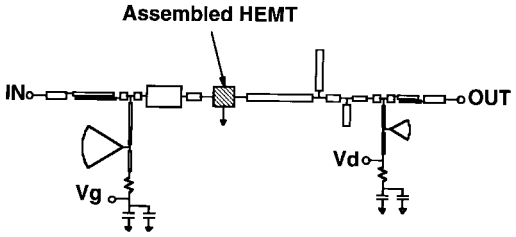


Fig. 12. Circuit diagram of 30/60-GHz frequency doubler.

metal. Ground patterns on the surface have been connected to the backside metal layer of the substrate with via-holes of 200-μm diameter.

Stud bumps were fabricated on the HEMT chip. The size of as-assembled gold bumps for flip-chip assembly was chosen based on the previously presented analytical results, with the height of 30 μm and the diameter of 80 μm. These dimensions are also advantageous in terms of process simplicity because conventional bump fabricating processes are applicable.

A two-stage cascade amplifier and frequency doubler operating at 60 GHz were developed with this MIC structure.

C. Two-Stage Amplifier

Fig. 9 shows a circuit diagram of the two-stage cascade amplifier. The circuit design was carried out first with small-signal simulation and succeeding optimization through harmonic-balance simulation. This amplifier includes input, output, and interstage matching circuits consisting of microstrip lines and open stubs. Coupled lines are employed for dc blocking in the input, output, and interstage circuits. Gate and drain bias voltages are supplied through bias circuits consisting of quarter-wavelength high-impedance lines and radial stubs providing band rejection at 60 GHz.

Fig. 10 shows a comparison of small-signal S-parameters for the amplifier measured with a network analyzer and theoretical values from the circuit simulator. Input power of the network analyzer data was -20 dBm. The drain bias level was $V_{\rm d1} = V_{\rm d2} = 2$ V. Gate bias levels were tuned so that dc drain currents for each stage would be $I_{\rm d1} = I_{\rm d2} = 10$ mA. Measured small-signal gain (S_{21}) larger than 10 dB is obtained in the frequency region from 55.4 to 64.0 GHz. The maximum value of S_{21} is 12.8 dB at 58.6 GHz. Measured and simulated results for all four S-parameters exhibit very similar frequency characteristics, supporting the validity of the design method.

The power performance measured at 60 GHz is presented in Fig. 11. Here the drain bias voltage was 3 V. The output power at 1-dB gain compression point ($P_{1\,\rm dB}$) is 12.9 dBm. At this $P_{1\,\rm dB}$ condition, the total drain current for the amplifier is 28.5 mA and power-added efficiency is 20.4%.

D. Frequency Doubler

Fig. 12 shows a circuit diagram of the 30/60-GHz frequency doubler. The input matching circuit is designed for the fundamental frequency and consists of quarter-wavelength microstrip lines as an impedance transformer. The output matching circuit for the second harmonic includes an open stub and microstrip line. A quarter-wavelength open stub as a band-rejection filter for the fundamental and the third harmonic frequency is also introduced on the output side of the HEMT. The frequency doubler was primarily designed using small-signal simulation. Succeeding harmonic-balance simulation was then carried out to optimize the load to achieve maximum conversion gain. A drain voltage of 2 V and drain current of 0.2 mA near pinchoff were chosen as the operating point for the circuit design. Fig. 13 shows the measured and simulated characteristics of the frequency doubler. The input power is 0.4 dBm. Similar frequency trends between measured and simulated results can be observed. Maximum conversion gain is 0.4 dB at an input frequency of 30.4 GHz. The fundamental suppression ratio at the maximum gain is

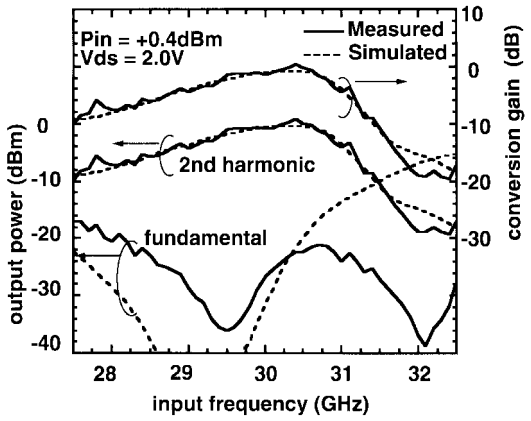


Fig. 13. Measured and simulated characteristics of 30/60-GHz frequency doubler.

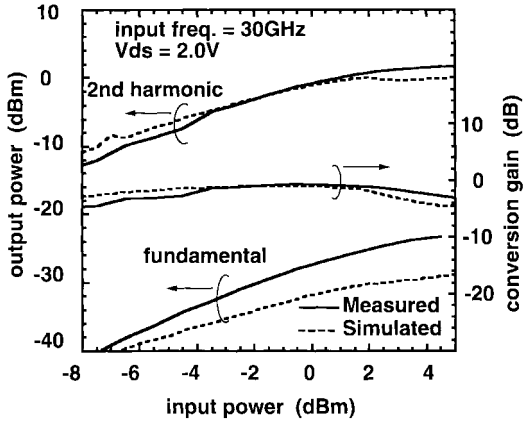


Fig. 14. Power characteristics of 30/60-GHz frequency doubler.

−23.0 dB. Optimum frequency conditions for fundamental suppression and for conversion gain are slightly different: the maximum fundamental suppression of −35 dB occurs when the input frequency is 29.5 GHz, where the conversion gain has decreased to −1.44 dB. The frequency range over which the conversion gain is greater than −3 dB is from 29.4 to 30.9 GHz.

The power performance at an input frequency of 30 GHz is shown in Fig. 14. The conversion gain versus input power has a very broad characteristic; e.g., variation of input power from −5.5 to +5.0 dBm results in a small conversion gain deviation from −3.0 to −0.7 dB.

IV. Conclusion

Through 3-D electromagnetic-field analysis of the flip-chip assembled structure, parasitics due to assembly, including chip–substrate electromagnetic interaction, have been accurately analyzed. An equivalent circuit for the flip-chip assembled 0.10-μm-gate p-HEMT has been derived from the results of field analysis. A bump height of 30 μm was chosen to suppress the chip–substrate effect and minimize the sensitivity of the assembly parasitics to bump height variation. This dimension is also advantageous because of the process simplicity, since conventional bump fabricating processes are applicable.

Two-stage amplifier and frequency-doubler MIC's in 60-GHz band were designed with the flip-chip assembled p-HEMT.

The amplifier has a maximum small-signal gain of 12.8 dB. The gain is greater than 10 dB from 55.4 to 64.0 GHz. At 60 GHz, 1-dB gain compression power of 12.9 dBm with power-added efficiency of 20.4% are obtained.

The frequency doubler has a maximum conversion gain of 0.4 dB. The fundamental suppression ratio at the maximum gain point is −23.0 dB. A conversion gain better than −3 dB is obtained for a wide range of input power from −5.5 to +5.0 dBm.

These circuits exhibited fairly high performance for 60-GHz MIC's. Furthermore, the observed frequency behavior of the MIC's are similar to that predicted by the simulations. This fact suggests that the design method demonstrated in this paper is fully adequate for millimeter-wave MIC's. The good agreement between the measured and simulated frequency characteristics for both circuits is clear evidence of the validity of the design method.

We conclude that the flip-chip assembled MIC approach presented in this paper has great potential for future millimeter-wave applications.

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